

# Compendium of Test Results of Single Event Effects Conducted by the Jet Propulsion Laboratory

Gregory R. Allen, *Member, IEEE*

**Abstract**—This paper reports heavy ion and proton induced single event effects results for a variety of microelectronic devices targeted for possible use in NASA spacecrafsts. The compendium covers a sampling of devices tested over the past eight years.

**Index Terms**—Single Event Effects, compendium, analog switches, ADC, DAC, oscillators, SDRAM, FPGA, drivers, microprocessors, voltage comparator, and voltage regulator.

## I. INTRODUCTION

The use of microelectronics in spacecraft and satellites requires those devices preserve their functionality in harsh radiation environments found in space. To ensure both the reliability and functionality of those devices, ground based testing to define microelectronic susceptibility to single event effects (SEE) remains important. The data presented in this paper were acquired to characterize the susceptibility of potential spacecraft microelectronics to single event latchup (SEL), single event upset (SEU), single event functional interrupt (SEFI), and single event transient (SET). This compendium represents SEE data acquired by the Jet Propulsion Laboratory radiation group from February 2000 to February 2008.

## II. EXPERIMENTAL PROCEDURE

### A. Test Facilities

A variety of ion facilities are available for experimental use. The criterion to select a test facility may include: scheduling, ion range, and/or programmatic expense. A high level view of the facilities used is outlined below. The facility websites [1]-[4], [26], and [27] provide a detailed view of available ions, energies, and facility capabilities that are beyond the scope of this paper.

#### 1) Heavy Ion Facilities

Heavy ion measurements were performed at either Brookhaven National Laboratory (BNL), the Lawrence Berkeley National Laboratory (LBNL) 88 inch cyclotron, or at the Texas A&M University Cyclotron (TAM). The BNL facility uses a twin Tandem Van De Graaff accelerator and the LBNL and TAM facilities use an 88 inch cyclotron. Both of these facilities are capable of diverse range of particle beams and energies for radiation effects testing. The longer-range ions at TAM allow much of the irradiations to be performed in air, whereas all testing at BNL took place in vacuum. Intermediate LETs were acquired either through the use of degrader (TAM) or by changing the angle of incidence of the ion relative to the device under test (DUT), providing an effective LET.

#### 2) Proton and Neutron Facilities

Proton tests were performed at the University of California, Davis (UCD) Crocker Nuclear Laboratory (CNL) or at the Indiana University Cyclotron Facility (IUCF). Much of the work associated with recent proton testing has been relegated to displacement damage effects, and have not been included in this paper. The majority of the representative proton data in this compendium has complimentary heavy ion data, and was acquired to achieve rates for particular environments. Neutron testing was performed at the Boeing Radiation Effects Laboratory (BREL). BREL uses a Kaman Sciences A711 neutron generator that produces a 14 MeV neutron beam.

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G. R. Allen is with the Jet Propulsion Laboratory (JPL), 4800 Oak Grove Dr., MS 303-220, Pasadena, CA 91109 USA (telephone: 818-393-7558, e-mail: [gregory.r.allen@jpl.nasa.gov](mailto:gregory.r.allen@jpl.nasa.gov)).

The following is a list of contact information for principle investigators of the data represented in this document:

Heidi N. Becker, Mohamed Elghafari, Steven M. Guertin, Farokh Irom, Allan H. Johnston, Tetsuo F. Miyahira, Duc N. Nguyen, and Joe N. Solario are with JPL, 4800 Oak Grove Dr., Pasadena, CA, 91109. H. Becker phone: 818-393-5491, email: [Heidi.N.Becker@jpl.nasa.gov](mailto:Heidi.N.Becker@jpl.nasa.gov); M. Elghafari phone: 818-393-7525, email: [Mohamed.Elghafari@jpl.nasa.gov](mailto:Mohamed.Elghafari@jpl.nasa.gov); S. Guertin phone: 818-393-6895, email: [Steven.M.Guertin@jpl.nasa.gov](mailto:Steven.M.Guertin@jpl.nasa.gov); F. Irom phone: 818-354-7463, email: [Farokh.Irom@jpl.nasa.gov](mailto:Farokh.Irom@jpl.nasa.gov); A. Johnston phone: 818-354-6425, email: [Allan.H.Johnston@jpl.nasa.gov](mailto:Allan.H.Johnston@jpl.nasa.gov); T. Miyahira phone: 818-354-2908, email: [Tetsuo.F.Miyahira@jpl.nasa.gov](mailto:Tetsuo.F.Miyahira@jpl.nasa.gov); D. Nguyen phone: 818-354-8554, email: [Duc.N.Nguyen@jpl.nasa.gov](mailto:Duc.N.Nguyen@jpl.nasa.gov).

Jeffery D. Patterson, formally of JPL, is now with Lockheed Martin (email: [Jeffrey.d.patterson@lmco.com](mailto:Jeffrey.d.patterson@lmco.com)).

Gary M. Swift, formally of JPL, is now with Xilinx Inc., San Jose, CA 95124 CA USA. (telephone: 408-879-2751, email: [gswift@xilinx.com](mailto:gswift@xilinx.com)).

### B. Experimental Methods

Details concerning experimental methodology including data acquisition, ion selection, biasing conditions, etc. vary from experimenter to experimenter and device to device. In many instances devices were tested both at room temperature and at elevated temperature; results are shown for both instances. Generally speaking, approaches used by experimenters followed the procedures documented in the ASTM F1192 or JEDEC JESD57 standards for single event testing [5], [6]. For details concerning the specifics of a test, please review the associated test report.

### III. DATA ORGANIZATION

This compendium is intended to serve as a reference list for tested devices. The data tables contain abbreviated information mainly due to spatial constraints. It is highly recommended that the reader review the referenced article or contact the principle investigator (PI) to acquire details concerning the data and test methodologies. Much of the SEE data presented here is dependent on the device's bias and circuit configuration; e.g. SET data depends strongly on its output load; SEFI data is interpretive depending upon what the test defines as a SEFI. Generally speaking, the worst-case results are presented, but it is highly recommended that the reader seek out the test report. Unfortunately, much of the data currently exists as internal documentation, represented by an 'I' in the reference column. We are currently working to get the data/reports released to the JPL parts radiation database [27].

When possible LET thresholds were shown to lie between a set of tested energies, otherwise they are simply shown to be at or below a certain value or not seen at the highest tested LET. SEE results have been combined on a single line. For most SEL results, only the thresholds have been provided. Saturated cross-sections and thresholds are provided for SEFI, SEU, and SET where available. Unless otherwise noted, all LET values are in MeV•cm<sup>2</sup>/mg and all cross-sections in cm<sup>2</sup>/device.

Acronyms, abbreviations, and conventional symbol use are shown in Table I, abbreviations for PIs are shown in Table II, and results are shown in Table III.

TABLE I  
ACRONYMS, ABBREVIATIONS, AND CONVENTIONAL SYMBOLS

ABBREVIATION	DEFINITION
ADC	ANALOG TO DIGITAL CONVERTER
ADI	ANALOG DEVICES, INC.
ASIC	APPLICATION-SPECIFIC INTEGRATED CIRCUIT
CMOS	COMPLEMENTARY METAL OXIDE SEMICONDUCTOR
CPU	CENTRAL PROCESSING UNIT
D-CACHE	DATA CHACHE
DAC	DIGITAL TO ANALOG CONVERTER
DRAM	DYNAMIC RANDOM ACCESS MEMORY
DSP	DIGITAL SIGNAL PROCESSOR
DUT	DEVICE UNDER TEST
FPGA	FIELD PROGRAMMABLE GATE ARRAY

FPR	FLOATING POINT REGISTER
GPR	GENERAL PURPOSE REGISTER
H	HEAVY ION TEST
I	INTERNAL DOCUMENT (CONTACT PI FOR SOURCE DATA)
I/O	INPUT/OUTPUT
IBM	INTERNATIONAL BUSINESS MACHINE
LET	LINEAR ENERGY TRANSFER (MeV•cm <sup>2</sup> /mg)
LET <sub>TH</sub>	LINEAR ENERGY TRANSFER THRESHOLD
LTN	LINEAR TECHNOLOGY
MOSFET	METAL OXIDE SEMICONDUCTOR FIELD EFFECT TRANSISTOR
MSK	MS KENNEDY
MUX	MUXPLEXOR
N	NEUTRON TEST
NAND	NOT AND LOGICAL OPERATION
OP AMP	OPERATIONAL AMPLIFIER
P	PROTON TEST
PI	PRINCIPLE INVESTIGATOR
PLL	PHASE LOCKED LOOP
σ	CROSS-SECTION
σ <sub>SAT</sub>	SATURATED CROSS-SECTION
SDRAM	SYNCHRONOUS DYNAMIC RANDOM ACCESS MEMORY
SEE	SINGLE EVENT EFFECT
SEFI	SINGLE EVENT FUNCTIONAL INTERRUPT
SEL	SINGLE EVENT LATCHUP
SET	SINGLE EVENT TRANSIENT
SEU	SINGLE EVENT UPSET
SPR	SPECIAL PURPOSE REGISTER
TI	TEXAS INSTRUMENTS
TLB	TRANSLATION LOOKASIDE BUFFER

TABLE II  
LIST OF PRINCIPLE INVESTIGATORS

PRINCIPAL INVESTIGATOR	ABBREVIATION
GREG ALLEN	GA
HEIDI BECKER	HB
MOHAMED ELGHEFARI	ME
STEVE GUERTIN	SG
FAROKH IROM	FI
ALLAN JOHNSTON	AJ
TETSUO MIYAHIRA	TM
DUC NGUYEN	DN
JEFF PATTERSON	JP
GARY SWIFT	GS

#### IV. TEST RESULTS

TABLE III  
SEE RESULTS

P.I.	Date	Device	Function	Mfr.	Technology	Test Type	Test Facility	Test Results	Ref.
<b>Analog Switches/MUXs</b>									
FI	Aug, 2007	HI-507	Analog MUX	Intersil	CMOS	SEL	TAM	LET <sub>th</sub> >85.4 @ 85°C	I
TM	Apr, 2001	ADG411	Analog Switch	ADI	CMOS	SEL	BNL	52 < LET <sub>th</sub> <= 52.6 @ 25°C	I
FI	Feb, 2005	DG202AEUE	Analog switch	Maxim	CMOS	SEL	TAM	LET <sub>th</sub> > 84.7 @ 125°C	I
FI	Aug, 2004	DG412AK	Analog switch	Maxim	CMOS	SEL	TAM	LET <sub>th</sub> > 86.3 @ 125°C	[8]
FI	Aug, 2004	DG413AK	Analog switch	Maxim	CMOS	SEL	TAM	LET <sub>th</sub> > 86.3 @ 125°C	[8]
FI	Oct, 2007	ISL43110	Analog switch	Intersil	CMOS	SEL	TAM	LET <sub>th</sub> > 85.4 @ 85°C	I
<b>ADC (10-bit)</b>									
LS	Jun, 2006	AD9731	10-bit ADC	ADI	Bipolar	SEL	TAM	LET <sub>th</sub> >75 @ 85°C	I
<b>ADC (12-bit)</b>									
LS	Nov, 2003	AD1672	12-bit ADC	ADI	BiCMOS	SEL	TAM	LET <sub>th</sub> > 120 @ 25°C	I
TM	Aug, 2000	AD9042	12-bit ADC	ADI	Bipolar	SEL	BNL	LET <sub>th</sub> >119 @ 25°C	I
LS	Nov, 2001	LTC1409	12-bit ADC	LTN	CMOS	SEL	TAM	LET <sub>th</sub> > 120 @ 25°C	I
<b>ADC (14-bit)</b>									
GS	Jun, 2000	AD9240	14-bit ADC	ADI	CMOS	SEL	TAM	LET <sub>th</sub> < 16.2 @ 25 °C	[18]
TM	Jun, 2002	AD9244	14-bit ADC	ADI	CMOS	SEL	BNL	LET <sub>th</sub> < 12.9 @ 25 °C	I
TM	Aug, 2003	LTC1417	14-bit ADC	LTN	CMOS	SEL	TAM	80.7 < LET <sub>th</sub> < 90 @ 82°C	I
FI	Mar, 2007	LTC1419AIG	14-bit ADC	LTN	CMOS	SEL	TAM	64 < LET <sub>th</sub> < 68.3 @ 85°C	I
<b>ADC (16-bit)</b>									
FI	Dec, 2004	AD977	16-bit ADC	ADI	BiCMOS	SEL	BNL	LET <sub>th</sub> > 84 @ 85°C	[7]
LS	Nov, 2001	ADS7809	16-bit ADC	Burr Brown	CMOS	SEL	TAM	19 < LET <sub>th</sub> < 22 @ 25°C	I
FI	Apr, 2004	LTC1609	16-bit ADC	LTN	CMOS	SEL	BREL	$\sigma_{\text{sat}} \sim 1.6 \times 10^{-10}$ @ 14 MeV	[23]
FI	Sep, 2006	LTC1609	16-bit ADC	LTN	CMOS	SEL	TAM, BNL	5.26 < LET <sub>th</sub> < 7.97 @ 85°C	I
FI	Apr, 2006	LTC1604	333ksps, 16-bit ADC	LTN	CMOS	SEL	TAM	63 < LET <sub>th</sub> < 65 @ 23°C 55 < LET <sub>th</sub> < 58 @ 85°C	[8]
FI	Sep, 2004	LTC1609	200ksps, 16-bit ADC	LTN	CMOS	SEL	BNL, TAM	8 < LET <sub>th</sub> < 11.7 @ 25°C 5.3 < LET <sub>th</sub> < 8 @ 85°C	[8]
FI	Dec, 2004	LTC1864	16-bit ADC	LTN	CMOS	SEL	BNL, TAM	LET <sub>th</sub> < 8.5 @ 25°C $\sigma_{\text{sat}} \sim 1.3 \times 10^{-2}$ @ LET 53	[8]
<b>ADC (24-bit)</b>									
LS	Jul, 2006	AD7714	24-bit ADC	ADI	BiCMOS	SEL	TAM	LET <sub>th</sub> < 27.1 @ 25°C LET <sub>th</sub> < 19 @ 85°C	I

P.I.	Date	Device	Function	Mfr.	Technology	Test Type	Test Facility	Test Results	Ref.
<b>Clocks/PLLs/Oscillators</b>									
TM	Nov, 2002	CPPC7L-BP-1.2TS	Oscillator	Cardinal	CMOS	SEL	TAM	LET <sub>th</sub> < 14 @ 40°C LET <sub>th</sub> < 19 @ 25 °C	I
TM	Nov, 2002	TCXO-5x7-12.0MHZ	Oscillator	Cardinal	CMOS	SEL	TAM	LET <sub>th</sub> < 19 @ 25°C	I
LS	Feb, 2005	VPC1-E3F	Oscillator	VITE Tech	CMOS	SEL	TAM	LET <sub>th</sub> > 86.3 @ 85°C	[8]
FI	Nov, 2007	CD54HCT4046	Phase -Locked Loop	TI	CMOS	SEL	TAM	LET <sub>th</sub> > 85 @ 25°C 69.1 < LET <sub>th</sub> < 73.0 @ 60°C 51.5 < LET <sub>th</sub> < 69.1 @ 125°C	I
FI	Apr, 2007	CDCV855	PLL clock	TI	CMOS	SEL	BNL	LET <sub>th</sub> > 52.9 @ 65°C LET <sub>th</sub> < 37.5 @ 85°C	I
FI	Apr, 2007	CY22392	PLL clock	Cypress	CMOS	SEL	BNL	LET <sub>th</sub> > 52.9 @ 85°C	I
<b>DAC (8-bit)</b>									
LS	May, 2000	X9C503	8-bit DAC	Xicor	CMOS	SEL	TAM	LET <sub>th</sub> < 22 @ 25°C	[22]
<b>DAC (12-bit)</b>									
LS	May, 2000	AD8420	12-bit DAC	Analog Devices	CMOS	SEL	TAM	LET <sub>th</sub> > 120 @ 25°C	[22]
LS	Nov, 2001	AD7541	12-bit DAC	Harris	BiCMOS	SEL	TAM	LET <sub>th</sub> > 75 @ 25°C	I
ME	Feb, 2006	AD7245A	12-bit DAC	ADI	BiCMOS	SEL	TAM	70.0 < LET <sub>th</sub> < 75 @ 25°C	I
LS	May, 2000	MAX539	12-bit DAC	Maxim	CMOS	SEL	TAM	LET <sub>th</sub> > 120 @ 25°C	[22]
<b>DAC (16-bit)</b>									
FI	Apr, 2004	LTC1595	16-bit DAC	LTN		SEL	BNL	10 < LET <sub>th</sub> < 11.7 @ 25°C 8 < LET <sub>th</sub> < 10 @ 85°C	[8]
LS	May, 2000	AD768	16 Bit DAC	Analog Devices	ABCMOS	SEL	TAM	LET <sub>th</sub> > 120 @ 25°C	[22]
TM	Aug, 2003	LTC1650	16-bit DAC	Linear Tech		SEL	TAM	LET <sub>th</sub> < 27 @ 82°C	I
<b>DSP</b>									
DN	Apr, 2001	ADSP-2100	DSP	ADI	CMOS	SEL	BNL	LET <sub>th</sub> < 11.4 @ 25°C	I
ME	Apr, 2007	ADSP-BF533	DSP	ADI	CMOS	SEL	BNL	LET <sub>th</sub> < 15 @ 25°C	I
<b>FPGAs</b>									
GA	Sep, 2005	Stratix-II	FPGA	Altera	CMOS	SEL	TAM	LET <sub>th</sub> < 3 @ 25°C SEL $\sigma_{sat} \sim 1.3 \times 10^{-2}$ @ LET 53	[11]
GA	Oct, 2005	ProAsic Plus	FPGA	Actel	CMOS	SEU	TAM	LET <sub>th</sub> < 3	[11]
GS	Jun, 2005	Virtex-II	FPGA	Xilinx	CMOS	SEU/SEL/SEFI	TAM	SEL LET <sub>th</sub> > 160 @ 120°C SEU/SEFI LET <sub>th</sub> < 1 SEU $\sigma_{sat}/bit \sim 4.37 \times 10^{-8}$ @ LET 60 SEFI $\sigma_{sat} \sim 4.47 \times 10^{-6}$ @ LET 90	[9]
GA	Aug, 2007	Virtex 4	FPGA	Xilinx	CMOS	SEL/SEU/SEFI	TAM	SEL LET <sub>th</sub> > 90 @ 120°C SEU/SEFI LET <sub>th</sub> < 1 SEU $\sigma_{sat}/bit \sim 4.37 \times 10^{-8}$ @ LET 108 SEFI $\sigma_{sat} \sim 6.4 \times 10^{-5}$ @ LET 90	[10]

P.I.	Date	Device	Function	Mfr.	Technology	Test Type	Test Facility	Test Results	Ref.
<b>Line Driver/Receiver/Transceiver</b>									
FI	Apr, 2007	UT63M147	1553A bus transceiver	Aeroflex	Bipolar	SEL/SET	TAM	SEL LET <sub>th</sub> > 77.3 @ 125°C SET LET <sub>th</sub> < 7 SET σ <sub>sat</sub> ~1.5x10 <sup>-5</sup> @ LET 60	I
FI	Jan, 2007	26CTLV31	Diff line driver	Intersil	CMOS	SET	BNL	LET <sub>th</sub> > 59.7	I
FI	Mar, 2007	SN55LBC174	Diff line driver	TI	BiCMOS	SEL/SET	TAM	SEL LET <sub>th</sub> > 68.3 @ 25°C SET LET <sub>th</sub> < 2.7 SET σ <sub>sat</sub> ~1x10 <sup>-4</sup> @ LET 70	I
FI	Jan, 2007	26CLV32RH	Diff line receiver	Intersil	CMOS	SET	BNL	LET <sub>th</sub> < 20 σ <sub>sat</sub> ~1.5x10 <sup>-5</sup> @ LET 60	I
FI	Jan, 2007	26CT32RH	Diff line receiver	Intersil	CMOS	SET	BNL	SET LET <sub>th</sub> < 20 SET σ <sub>sat</sub> ~5x10 <sup>-6</sup> @ LET 60	I
FI	Mar, 2007	SN55LBC175	Diff line receiver	TI	BiCMOS	SEL/SET	TAM	SEL LET <sub>th</sub> > 68.3 @ 25°C SET LET <sub>th</sub> < 2.7 SET σ <sub>sat</sub> ~1x10 <sup>-4</sup> @ LET 70	I
LS	Jul, 2006	SEN-5588	MOSFET drivers	Sensitron	CMOS	SEL	TAM	LET <sub>th</sub> < 25 @ 25°C	I
TM	Aug, 2000	LTC1157	Driver, MOSFET	LTN	CMOS	SEL	BNL	LET <sub>th</sub> > 120 @ 25°C	I
FI	Nov, 2004	TC4423	Driver, MOSFET	Microchip	CMOS	SEL	BNL, TAM	LET <sub>th</sub> > 86.3 @ 125°C	[8]
<b>Logic Devices</b>									
FI	Apr, 2007	NCS7S08	AND gate	Fairchild	CMOS	SEL	BNL	LET <sub>th</sub> > 52.9 @ 85°C	I
FI	Apr, 2007	CDCV304	Clock buffer	TI	CMOS	SEL	BNL	LET <sub>th</sub> > 52.9 @ 25°C LET <sub>th</sub> < 52.9 @ 65°C σ <sub>sat</sub> ~2.2x10 <sup>-6</sup> @ LET 52.9, 65°C	I
FI	Jun, 2007	SN54LVTH244	Octal buffer	TI	BiCMOS	SEL/SET	TAM	SEL LET <sub>th</sub> > 77.3 @ 25°C SET 9.6 < LET <sub>th</sub> < 15.0 SET σ <sub>sat</sub> ~8.2x10 <sup>-5</sup> @ LET 77.3	I
FI	Dec, 2004	CY23FS08	Failsafe buffer	Cypress	CMOS	SEL/SEU	BNL, TAM	55 < SEL LET <sub>th</sub> < 70 @ 85°C SEU LET <sub>th</sub> < 8.5	[8]
<b>Microprocessor (32-bit)</b>									
GS	Nov, 2001	PPC750	CPU	IBM	CMOS	SEU	TAM	SPR SEU LET <sub>th</sub> < 6 SPR SEU σ <sub>sat</sub> /bit~6x10 <sup>-8</sup> @ LET 46 FPR SEU LET <sub>th</sub> < 6 FPR SEU σ <sub>sat</sub> /bit~3.5x10 <sup>-7</sup> @ LET 54	[12]
GS	May/Jun, 2001	PPC750	CPU	IBM	CMOS	SEU	UCD/IUCF	D-Cache SEU Energy <sub>th</sub> < 15 D-Cache σ <sub>sat</sub> /bit~5x10 <sup>-14</sup> @ 200MeV	[12]

P.I.	Date	Device	Function	Mfr.	Technology	Test Type	Test Facility	Test Results	Ref.
GS	Nov, 2001	XPC750	CPU	Motorola	CMOS	SEU	TAM	SPR SEU $\text{LET}_{\text{th}} < 6$ SPR SEU $\sigma_{\text{sat}}/\text{bit} \sim 1 \times 10^{-7}$ @ LET 60 FPR SEU $\text{LET}_{\text{th}} < 4$ FPR SEU $\sigma_{\text{sat}}/\text{bit} \sim 2 \times 10^{-7}$ @ LET 60	[12]
GS	May/Jun, 2001	XPC750	CPU	Motorola	CMOS	SEU	UCD/IUCF	FPR SEU Energy $_{\text{th}} < 20$ FPR $\sigma_{\text{sat}}/\text{bit} \sim 1 \times 10^{-13}$ @ 200 MeV D-Cache SEU Energy $_{\text{th}} < 10$ D-Cache $\sigma_{\text{sat}}/\text{bit} \sim 6 \times 10^{-14}$ @ 200 MeV	[12]
FI	Jun, 2001	PowerPC 7455	CPU	Motorola	CMOS	SEU	IUCF	TLB SEU Energy $_{\text{th}} < 20$ TLB $\sigma_{\text{sat}}/\text{bit} \sim 1 \times 10^{-14}$ @ 63 MeV	[13]
FI	Jul, 2001	PowerPC 7455	CPU	Motorola	CMOS	SEU	TAM	D-Cache SEU $\text{LET}_{\text{th}} < 1.36$ D-Cache SEU $\sigma_{\text{sat}}/\text{bit} \sim 2.7 \times 10^{-9}$ @ LET 25 TLB SEU $\text{LET}_{\text{th}} < 1$ TLB SEU $\sigma_{\text{sat}}/\text{bit} \sim 4 \times 10^{-9}$ @ LET 25 FPR SEU $\text{LET}_{\text{th}} < 1$ FPR SEU $\sigma_{\text{sat}}/\text{bit} \sim 1 \times 10^{-8}$ @ LET 25	[13]
FI	Jun, 2001	PowerPC 750Fx	CPU	IBM	CMOS	SEU	IUCF	D-cache SEU Energy $_{\text{th}} < 20$ D-cache $\sigma_{\text{sat}}/\text{bit} \sim 1 \times 10^{-14}$ @ 63 MeV	[13]
FI	Jul, 2001	PowerPC 750Fx	CPU	IBM	CMOS	SEU	TAM	D-Cache SEU $\text{LET}_{\text{th}} < 1$ D-Cache SEU $\sigma_{\text{sat}}/\text{bit} \sim 2 \times 10^{-9}$ @ LET 25 FPR SEU $\text{LET}_{\text{th}} < 1$ FPR SEU $\sigma_{\text{sat}}/\text{bit} \sim 7 \times 10^{-9}$ @ LET 19	[13]
FI	Dec, 2002	PowerPC 7457	CPU	Motorola	CMOS	SEU	TAM	D-cache SEU $\text{LET}_{\text{th}} < 2$ D-cache $\sigma_{\text{sat}}/\text{bit} \sim 3 \times 10^{-9}$ @ LET 15	[14]
FI	Sep, 2006	PowerPC 7447	Power PC	Motorola	CMOS	SEU	BREL	SEU $\sigma_{\text{sat}}/\text{bit} \sim 1.3 \times 10^{-14}$ @ 14 MeV SEFI $\sigma_{\text{sat}} \sim 2.7 \times 10^{-10}$ @ 14 MeV	[23]
FI	Aug, 2006	PowerPC 7448	Power PC	Motorola	CMOS	SEU/SEFI	TAM	D-cache SEU $\text{LET}_{\text{th}} < 2$ D-cache SEU $\sigma_{\text{sat}}/\text{bit} \sim 1.1 \times 10^{-9}$ Hangs SEFI $\text{LET}_{\text{th}} < 2$ Hangs SEFI $\sigma_{\text{sat}} \sim 1 \times 10^{-5}$ @ LET 14	[15]
FI	Feb, 2006	SPARCTSC695F	Processor	Atmel	CMOS	SEU/SEL	TAM	SEL $\text{LET}_{\text{th}} > 109.7$ @ 25°C SEU $\text{LET}_{\text{th}} < 15$ SEU $\sigma_{\text{sat}} \sim 9 \times 10^{-6}$ @ LET 30	I
<b>Miscellaneous</b>									
LS	Dec, 2000	X9C503	Potentiometer	Xicor	CMOS	SEL	TAM	$\text{LET}_{\text{th}} < 22$ @ 25°C	I
SE	Feb, 2006	AD7750	Product to freq converter	ADI	CMOS	SEL	TAM	$10 < \text{LET}_{\text{th}} < 20$ @ 25°C $5 < \text{LET}_{\text{th}} < 10$ @ 85°C	I
FI	Apr, 2007	LTC1387	RS-232/485 Transceiver	LTN	CMOS	SEL	BNL	$\text{LET}_{\text{th}} > 52.9$ @ 85°C	I
SE	Apr, 2007	ADV7183B	SDTV video decoder	ADI	CMOS	SEL	BNL	$\text{LET}_{\text{th}} < 3.37$ @ 25°C	I

P.I.	Date	Device	Function	Mfr.	Technology	Test Type	Test Facility	Test Results	Ref.
<b>Miscellaneous</b>									
FI	Apr, 2007	LTC1772	Step down controller	LTN	CMOS	SEL	BNL	LET <sub>th</sub> > 52.9 @ 85°C	I
FI	Nov, 2005	MAX708	Supervisory circuit	Maxim	CMOS	SEL	TAM	72 < LET <sub>th</sub> < 75 @ 25°C LET <sub>th</sub> < 68 @ 85°C	[7]
FI	Sep, 2007	ADuM1401	Digital isolator	ADI	BiCMOS	SEL	BNL	LET <sub>th</sub> < 8.0 @ 25°C	I
FI	Apr, 2007	ADT7461A	Digital thermometer	ADI	CMOS	SEL	BNL	11.7 < LET <sub>th</sub> < 19.7 @ 25°C 8.0 < LET <sub>th</sub> < 11.7 @ 65°C	I
FI	Apr, 2007	DS1631	Digital thermometer	Maxim	CMOS	SEL	BNL	37.5 < LET <sub>th</sub> < 52.9 @ 25°C 26.6 < LET <sub>th</sub> < 52.9 @ 65°C	I
FI	Jun, 2005	TSS902E	Error Correc Decoder	Atmel	CMOS	SEL	TAM	LET <sub>th</sub> < 41 @ 125°C	[7]
FI	Dec, 2005	IDT72V36110	FIFO	IDT	CMOS	SEL	TAM	2.7 < LET <sub>th</sub> < 5 @ 80°C	[7]
SE	Feb, 2006	OMH3040	Hall effect sensor	Optec	Bipolar	SEU	TAM	LET <sub>th</sub> < 8 $\sigma_{sat} \sim 1 \times 10^{-3}$ @ LET 70	I
LS	Jun, 2004	AD9858	DDS	ADI	BiCMOS	SEU/SEL	TAM	SEU LET <sub>th</sub> < 7.5 SEU $\sigma_{sat} \sim 8.8 \times 10^{-5}$ @ LET 60 SEL LET <sub>th</sub> < 10 @ 25°C	[8]
SE	Apr, 2007	PSD4256G6V	Memory	ST	CMOS	SEL	BNL	LET <sub>th</sub> < 11 @ 25 °C	I
<b>Non-Volatile Memories</b>									
SE	Apr, 2007	AT25256AN	EEPROM	Atmel	CMOS	SEL	BNL	LET <sub>th</sub> > 37.45 @ 25°C	I
FI	Apr, 2007	MT29F2G08AABWP	Flash Memory	Micron	CMOS	SEU/SEFI	TAM	SEU/SEFI LET <sub>th</sub> < 5 SEU $\sigma_{sat}/bit \sim 1 \times 10^{-11}$ SEFI $\sigma_{sat} \sim 1 \times 10^{-5}$ @ LET 70	[24]
FI	Apr, 2007	MT29F4G08AAAWP	Flash Memory	Micron	CMOS	SEU/SEFI	TAM	SEU/SEFI LET <sub>th</sub> < 5 SEU $\sigma_{sat}/bit \sim 1 \times 10^{-11}$ SEFI $\sigma_{sat} \sim 1 \times 10^{-5}$ @ LET 70	[24]
FI	Apr, 2007	HY27UF084G2B	Flash Memory	Hynix	CMOS	SEU/SEFI	TAM	SEU/SEFI LET <sub>th</sub> < 5 SEU $\sigma_{sat}/bit \sim 1 \times 10^{-11}$ SEFI $\sigma_{sat} \sim 1 \times 10^{-5}$ @ LET 70	[24]
FI	Apr, 2007	NAND 90nm 2gb	Flash Memory	STMicro	CMOS	SEU/SEFI	TAM	SEU/SEFI LET <sub>th</sub> < 5 SEU $\sigma_{sat}/bit \sim 1 \times 10^{-11}$ SEFI $\sigma_{sat} \sim 1 \times 10^{-5}$ @ LET 70	[24]
FI	Apr, 2007	NAND 90nm 1gb	Flash Memory	Samsung	CMOS	SEU/SEFI	TAM	SEU/SEFI LET <sub>th</sub> < 5 SEU $\sigma_{sat}/bit \sim 1 \times 10^{-11}$ SEFI $\sigma_{sat} \sim 1 \times 10^{-5}$ @ LET 70	[24]
FI	Apr, 2007	NAND 90nm 2gb	Flash Memory	Samsung	CMOS	SEU/SEFI	TAM	SEU/SEFI LET <sub>th</sub> < 5 SEU $\sigma_{sat}/bit \sim 1 \times 10^{-11}$ SEFI $\sigma_{sat} \sim 1 \times 10^{-5}$ @ LET 70	[24]
FI	Apr, 2007	NAND 90nm 4gb	Flash Memory	Samsung	CMOS	SEU/SEFI	TAM	SEU/SEFI LET <sub>th</sub> < 5 SEU $\sigma_{sat}/bit \sim 1 \times 10^{-11}$ SEFI $\sigma_{sat} \sim 1 \times 10^{-5}$ @ LET 70	[24]

P.I.	Date	Device	Function	Mfr.	Technology	Test Type	Test Facility	Test Results	Ref.
LS	Jan, 2002	NAND 130nm 1Gb	Flash memory	Intel	CMOS	SEU/SEFI	TAM, LBNL	SEU/SEFI $\text{LET}_{\text{th}} < 7$ SEU $\sigma_{\text{sat}} \sim 1 \times 10^{-2}$ SEFI $\sigma_{\text{sat}} \sim 1 \times 10^{-1}$ @ LET 40	[19]
DN	Jan, 2002	NOR 130nm 256Mb	Flash Memory	StrataFlash	CMOS	SEL	TAM, LBNL	$\text{LET}_{\text{th}} < 5.64$ @ 25°C	[19]
FI	March, 2005	S29JL0643	Flash Memory	Spansion	CMOS	SEU/SEFI	BREL	SEU $\sigma_{\text{sat}}/\text{bit} \sim 2.9 \times 10^{-18}$ @ 14 MeV SEFI $\sigma_{\text{sat}} \sim 1.9 \times 10^{-10}$ @ 14 MeV	[23]
FI	March, 2006	S29JL0644	Flash Memory	Spansion	CMOS	SEU/SEFI	TAM	SEU/SEFI $\text{LET}_{\text{th}} < 8$ SEU $\sigma_{\text{sat}}/\text{bit} \sim 5.7 \times 10^{-12}$ SEFI $\sigma_{\text{sat}} \sim 3 \times 10^{-7}$	I
FI	Sep, 2006	K9F2G08U0M	Flash memory	Samsung	CMOS	SEU	BREL	SEU $\sigma_{\text{sat}}/\text{bit} \sim 1.1 \times 10^{-19}$ @ 14 MeV SEFI $\sigma_{\text{sat}} \sim 1.1 \times 10^{-10}$ @ 14 MeV	[23]
DN	Jun, 2004	K9F2G08U0M	Flash memory	Samsung	CMOS	SEFI	TAM	$\text{LET}_{\text{th}} < 2$ $\sigma_{\text{sat}} \sim 1 \times 10^{-3}$ @ LET 20	[21]
<b>Op Amps</b>									
FI	Apr, 2004	LTC2052	Opamp	LTN	CMOS	SEL	TAM	$\text{LET}_{\text{th}} < 5$ @ 82°C $\sigma_{\text{sat}} \sim 1 \times 10^{-4}$ @ LET 84.7	[16]
FI	Apr, 2004	LTC2052	Opamp	LTN	CMOS	SEL	BREL	$\sigma_{\text{sat}} \sim 1.6 \times 10^{-10}$ @ 14 MeV	[23]
TM	Dec, 2000	LMC6035	Opamp	NSC	CMOS	SEL	TAM	$\text{LET}_{\text{th}} > 100$ @ 25°C	I
TM	Apr, 2001	LMC6482	Opamp	NSC	CMOS	SEL	BNL	$\text{LET}_{\text{th}} > 99.24$ @ 25°C	I
TM	Dec, 2001	OP220	Opamp	ADI	Bipolar	SET	BNL	$\text{LET}_{\text{th}} < 3$ @ 25°C $\sigma_{\text{sat}} \sim 2 \times 10^{-3}$ @ LET 37	I
TM	Dec, 2001	OP27	Opamp	ADI	Bipolar	SET	BNL	$\text{LET}_{\text{th}} < 3$ @ 25°C $\sigma_{\text{sat}} \sim 6 \times 10^{-4}$ @ LET 37	I
LS	Apr, 2004	RH108AW	Opamp	LTN	Bipolar	SET	BNL	$\text{LET}_{\text{th}} < 1$ @ 25°C $\sigma_{\text{sat}} \sim 5 \times 10^{-3}$ @ LET 65	I
GS	Jun, 2003	TLC27M4	Opamp	TIX	LinCMOS	SEL	TAM	$\text{LET}_{\text{th}} > 80.2$ @ 92°C, 12V	I
FI	Oct, 2007	LMC6464	Quad Opamp	NSC	CMOS	SEL	TAM	$\text{LET}_{\text{th}} > 75$ @ 25°C	I
<b>Optoelectronics</b>									
FI	Apr, 2004	6N134	Optocoupler	Agilent	CMOS	SET	BREL	$\sigma_{\text{sat}} \sim 6.6 \times 10^{-8}$ @ 14 MeV	[23]
FI	Nov, 2007	HCPL-6250	Optocoupler	Agilent	CMOS	SET	TAM	$\text{LET}_{\text{th}} < 2.7$ $\sigma_{\text{sat}} \sim 4 \times 10^{-3}$ @ LET 85.4	I
<b>SRAM</b>									
LS	Feb, 2006	UT8Q512K8	SRAM	Aeroflex	CMOS	SEU	IUCF	SEU Energy <sub>th</sub> < 35 SEU $\sigma_{\text{sat}}/\text{bit} \sim 2.6 \times 10^{-15}$ @ 200 MeV	I
FI	Sep, 2006	UT8CR512K32	SRAM	Aeroflex	CMOS	SEU/SEL	BREL	SEU $\sigma_{\text{sat}}/\text{bit} \sim 3.9 \times 10^{-16}$ @ 14 MeV SEFI $\sigma_{\text{sat}} \sim 3.9 \times 10^{-10}$ @ 14 MeV	[23]
LS	Jan, 2002	WMS128k8	SRAM	White Electronics	CMOS	SEU/SEL	BNL	SEL $\text{LET}_{\text{th}} < 37$ @ 25°C SEU $\text{LET}_{\text{th}} < 1$ SEU $\sigma_{\text{sat}} \sim 7 \times 10^{-1}$ @ LET 50	I

P.I.	Date	Device	Function	Mfr.	Technology	Test Type	Test Facility	Test Results	Ref.
<b>SDRAM</b>									
SG	Dec, 2000	HY57V654020B	SDRAM	Hyundai	CMOS	SEU/SEL	TAM	LET <sub>th</sub> < 9.9 $\sigma_{sat} \sim 6 \times 10^{-5}$ @ LET 54	[20]
FI	Sep, 2006	K4S510432M	SDRAM	Samsung	CMOS	SEU/SEFI	BREL	SEU $\sigma_{sat}/bit \sim 1.7 \times 10^{-17}$ @ 14 MeV SEFI $\sigma_{sat} \sim 3.1 \times 10^{-10}$ @ 14 MeV	[23]
FI	Sep, 2006	MT48LC128M4A2	SDRAM	Micron	CMOS	SEU/SEFI	BREL	SEU $\sigma_{sat}/bit \sim 1.9 \times 10^{-17}$ @ 14 MeV SEFI $\sigma_{sat}/bit \sim 1.6 \times 10^{-9}$ @ 14 MeV	[23]
SE	Apr, 2007	MT48LC16M16A	SDRAM	Micron	CMOS	SEL	BNL	LET <sub>th</sub> < 25 $\sigma_{sat} \sim 1 \times 10^{-6}$	I
<b>Voltage Comparator</b>									
TM	May, 2002	AD790	Comparator	ADI	BiCMOS	SET	BNL	LET <sub>th</sub> < 1 @ $\Delta V_{in} = 50mV$ $\sigma_{sat} \sim 5 \times 10^{-5}$ @ LET 20	I
TM	May, 2002	CMP401	Comparator	ADI	BiCMOS	SET	BNL	LET <sub>th</sub> < 3 @ $\Delta V_{in} = 50mV$ $\sigma_{sat} \sim 1 \times 10^{-4}$ @ LET 20	I
TM	May, 2002	LM119	Comparator	NSC	Bipolar	SET	BNL	LET <sub>th</sub> < 6 @ $\Delta V_{in} = 50mV$ $\sigma_{sat} \sim 1 \times 10^{-4}$ @ LET 20	I
FI	Apr, 2004	LM139	Comparator	NSC	Bipolar	SET	BREL	$\sigma_{sat} \sim 1.6 \times 10^{-9}$ @ 14 MeV, $\Delta V_{in} = 20mV$	[23]
<b>Voltage Reference</b>									
FI	Aug, 2007	LM185	Voltage reference	NSC	Bipolar	SET	TAM	LET <sub>th</sub> < 3 @ 25°C $\sigma_{sat} \sim 1 \times 10^{-2}$ @ LET 51.5	I
<b>Voltage Regulator</b>									
FI	Jan, 2008	LM2941	Voltage regulator	NSC	Bipolar	SET	BNL	LET <sub>th</sub> < 1.4 $\sigma_{sat} \sim 1 \times 10^{-3}$ @ LET 40	I
FI	Jul, 2006	HS-117RH	Voltage regulator	Intersil	BiCOMS	SET	BNL, TAM	LET <sub>th</sub> < 2.7 $\sigma_{sat} \sim 5 \times 10^{-3}$ @ LET 68.3	[17]
AJ	Jun, 2006	LM117	Voltage regulator	NSC	Bipolar	SET	TAM	LET <sub>th</sub> < 3.7 $\sigma_{sat} \sim 5 \times 10^{-3}$ @ LET 80.1	[25]
FI	Sep, 2006	LM117HVH	Voltage regulator	NSC	Bipolar	SET	BREL	$\sigma_{sat} \sim 2.9 \times 10^{-10}$ @ 14 MeV	[23]
FI	Jun, 2006	LM137	Voltage regulator	NSC	Bipolar	SET	TAM, BNL	LET <sub>th</sub> < 3.7 $\sigma_{sat} \sim 6 \times 10^{-3}$ @ LET 26	[25]
FI	Oct, 2007	RH1085	Voltage regulator	LTN	Bipolar	SET	TAM	Contact PI	I
FI	Apr, 2007	LTC3413	Synchronous regulator	LTN	CMOS	SEL	BNL	11.7 < LET <sub>th</sub> < 19.7 @ 25°C, V <sub>CC</sub> =3.3 8.0 < LET <sub>th</sub> < 11.7 @ 65°C, V <sub>CC</sub> =3.3 LET <sub>th</sub> > 52.9 @ 65°C, V <sub>CC</sub> =2.5	I
FI	Jun, 2007	MSK5920-1.5RH	Voltage regulator	MSK	Hybrid	SET	TAM	Contact PI	I
FI	Jun, 2007	MSK5920-2.5RH	Voltage regulator	MSK	Hybrid	SET	TAM	Contact PI	I

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